ABSTRACT OF THE DISCLOSURE

A processor that includes an in-order execution architecture for executing at least two instructions per cycle (e.g., 2n instructions are processed per cycle, where n is an integer greater than or equal to one) and at least two symmetric execution units. The processor includes an instruction fetch unit for fetching n instructions (where n is an integer greater than or equal to one) and an instruction decoder for decoding the n instruction. The error detection mechanism includes duplication hardware for duplicating the n instructions into a first bundle of n instructions and a second bundle of n instructions. A first execution unit for executing the first bundle of instructions in a first execution cycle, and a second symmetric execution unit for executing the second bundle of instructions in the first execution cycle are provided. The error detection mechanism also includes comparison hardware for comparing the results of the first execution unit and the results of the second execution unit. The comparison hardware can have an exception unit for generating an exception (e.g., raising a fault) when the results are not the same. A commit unit is provided for committing one of the results when the results are the same.